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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,946	12/31/2003	Joon Bum Shim	040008-0305451	6221

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PILLSBURY WINTHROP, LLP
P.O. BOX 10500
MCLEAN, VA 22102

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 08/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,946	SHIM ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/31/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d).

Information Disclosure Statement

The information disclosure statement filed 12/31/03 has been considered.

Oath/Declaration

Oath/Declaration filed on 12/31/03 has been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 1 is objected because neither the specification nor the drawing provides the support for etching undercuts the polysilicon.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7-9, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunuma et al. (U.S. Publication No. 2004/0121593).

Referring to figures 1a-1F, Matsunuma et al. teaches a method of fabricating submicron semiconductor device comprising:

forming an oxide layer (12) on substrate (11);

forming a polysilicon layer (13) on said oxide layer;

forming a hard mask (14) on said polysilicon layer;

depositing a photoresist (15) on said hard mask and patterning said hard mask by using said photoresist (see figure 1b-1c); and

etching said polysilicon layer (13) using pattern embodied by said hard mask (14), wherein said etching undercuts said polysilicon layer to form a feature said polysilicon layer having critical dimension smaller than dimension in said hard mask (in view of the specification paragraph# 25, and figures 1-2, etching undercut the hardmask layer not the polysilicon layer).

Regarding to claim 7, The method according to claim 1, wherein said pattern embodied by said hard mask is formed by etching said hard mask using said photoresist patterned as an etching mask (see figures 1B-1C, paragraphs# 22-32).

Regarding to claim 8. wherein said hard mask is etched by means of isotropic etching (see paragraph# 27-32).

Regarding to claim 9, wherein said isotropic etching plasma etching (see paragraph# 27-32, ICP etching is plasma etch).

Regarding to claim 11, wherein said etching is performed through plasma etching (see paragraph# 27-32, ICP/ECR etching is plasma etch).

Regarding to claim 12, plasma etching performed using Cl_2/HBr, $C1_2/O_2$ or HBr/O_2 as an etching gas (see paragraphs# 22-43).

Claims 1-3, 7-8, 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Guo (U.S. Publication No. 2003/0211684).

Referring to figures 2-8, Guo teaches a method of fabricating submicron semiconductor device comprising:

forming an oxide layer (52) on substrate (10);

forming a polysilicon layer (54/56) on said oxide layer;

forming a hard mask (58) on said polysilicon layer;

forming an ARC layer (60) on the hard mask layer;

depositing a photoresist (62) on said hard mask and patterning said hard mask by using said photoresist (see figure 2-3); and

etching said polysilicon layer (54) using pattern embodied by said hard mask (58), wherein said etching undercuts said polysilicon layer to form a feature said polysilicon layer having critical dimension smaller than dimension in said hard mask (see figure 5).

Regarding to claim 2, The method according to claim 1, further comprising depositing an ARC (60) on said hard mask to lower corresponding critical reflectivity.

Regarding to claim 3, the method according to claim 2, the ARC is organic or inorganic material (60, SiN or SiON is inorganic).

Regarding to claim 7, The method according to claim 1, wherein said pattern embodied by said hard mask is formed by etching said hard mask using said photoresist patterned as an etching mask (see figures 3-4, paragraphs# 60-76).

Regarding to claim 8. wherein said hard mask is etched by means of isotropic etching (see paragraph# 73).

Regarding to claim 10, wherein said plasma etching uses SF_6 gas as an etching gas (see paragraph#73).

Regarding to claim 13, a method fabricating a submicron semiconductor device comprising:

forming an oxide layer (52) on a substrate (10);

forming a polysilicon layer (54/56) on said oxide layer;

forming a hard mask (58) on said polysilicon layer;

depositing a photoresist (62) on said hard mask and patterning said hard mask by using said photoresist (see figure 3-4); and

etching said polysilicon layer (54/56) using pattern embodied by said hard mask (58), and

selectively removing said hard mask (58) using a wet etch while protecting said polysilicon layer and said oxide layer from etching (see figure 6-7, paragraph# 73, 83).

Regarding to claim 14, hard mask so as comprising depositing an ARC on said to lower reflectivity (60, see figures 3-4, paragraph# 62-69).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4-6, 9-12, 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo (U.S. Publication No. 2003/0211684) as applied to claims 1-3, 7-8, 13-14 above in view of Matsunuma et al. (U.S. Publication No. 2004/0121593), Aminpur et al. (U.S. Patent No. 6,482,726), Wolf "silicon processing for the VLSI ERA" vol. 2, page 194, Bergman (U.S. Patent No. 5332445) and the Admitted Prior Art (pages 3-4).

Guo teaches forming a gate stack for CMOS devices by forming a silicon oxide, polysilicon, hardmask, antireflective layer, photoresist layer consecutively then pattern the layers. However, the reference does not teach forming a hardmask layer SiH_4 oxide deposited by PE-CVD, removing the hardmask layer by wet etching using HF gas and nitrogen gas, patterning the photoresist layer by using KRF layer as a light source, the etching rate, the percentage of HF, the temperature, etching selectivity, and the thickness or the hardmask layer.

Matsunuma et al. teaches hard mask is etched by means of isotropic etching plasma etching (see paragraph# 27-32, ICP/ECR etching is plasma etch), and plasma etching performed using Cl_2/HBr, $C1_2/O_2$ or HBr/O_2 as an etching gas (see paragraphs# 22-43).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etching or pattern the layer by using plasma etching in Cl_2/HBr, $C1_2/O_2$ or HBr/O_2 in process of Guo as taught by Matsunuma et al. because it is known in the art to provide a good selectivity, high uniformity of etching and easy to control the parameters during the etching process.

Aminpur et al. teaches forming a hardmask layer (650/740, silicon oxide) by using PECVD (see claims 1, 8), patterning the hardmask layer by isotropic etching or anisotropic etching using wet etching or plasma etching technique (see col. 7, lines 9-16, figures 6-7).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form hardmask layer by using PECVD, patterning the hardmask layer by isotropic etching or anisotropic etching using wet etching or plasma etching technique in process of Guo as taught by Aminpur et al. because forming the hardmask layer by PECVD process is known in the art to provide a good step coverage, patterning the layer by using isotropic etching or anisotropic etching using wet etching or plasma etching is known in the art to form a semiconductor devices with a critical dimension.

Wolf teaches forming the oxide layer by using silane (SiH4 gas) and O2 to form a silane-oxide layer by PECVD method (see table 4, page 194 of Wolf).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would from the silane-oxide layer by PECVD in process of

Guo as taught by Wolf because forming the PECVD oxide layer by using silane gas is known in the art to provide a good step coverage.

Bergman teaches etching the hardmask (oxide/nitride) layer by using HF and nitrogen gas (see col. 3, lines 41+, and col. 6, lines 15+).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etch the hardmask (oxide/nitride) layer by using HF and nitrogen gas in process of Guo et al. as taught by Bergman because the process would provide high speed etching of good uniformity and superior particle count performance.

The background of the invention teaches pattern the photoresist layer by using KrF laser as a light source (see paragraph# 8 of the present application).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would pattern the photoresist layer by using KrF laser as a light source in process of Guo et al. as taught by the background of the invention because the process is know to pattern the photoresist layer to achieve a high-integration semiconductor device.

The etching rate, the percentage of HF, the temperature, etching selectivity, and the thickness of the hardmask layer range of claims 6, 12, 15-18 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious:

> Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely

> degree from the results of the prior art...such ranges are termed □critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.□
> *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*
> Therefore, one of ordinary skill in the requisite art at the time the invention was made

would have used any etching rate, the percentage of HF, the temperature, etching selectivity, and the thickness range suitable to the method in process of Guo in order to optimize the process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN